Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An encoding and decoding process for a servo positioning system of a reading and writing head of a hard disk drive, comprising the following steps:

receiving a pattern signal that includes a plurality of groups of four bits;

encoding each group of four bits of the pattern signal in a Matched Spectral Null (MSN) format through an intermediate rate 4/6 code, thereby produced a six bit code word;

providing a duplicated bit for each bit of the six bit code word obtained with the previous step, thereby producing an encoded word ~~the~~ that is written to a hard disk of the hard disk drive;

reading a servo wedge information signal, that includes the encoded word, from the hard disk using a read and write channel of the hard disk drive; and

using a trellis Partial Response decoding scheme matched to said encoded word for obtaining angular and radial information for positioning the head.

2. (Original) The process according to claim 1 wherein the encoding phase is a concatenation of a 4/6 MSN encoding phase and a 1/2 repetition code.

3. (Currently Amended) The process according to claim 1 wherein a 'gray-like' code feature is achieved by imposing a property of a minimum Euclidean distance between code words corresponding to two consecutive gray codes.

4. (Original) The process according to claim 1 wherein the encoding step prevents MSN sequences such as '000111' and '111000' in order to minimize the number of trellis states.

5. (Original) The process according to claim 1 wherein a sixteen states Viterbi detector is used for the decoding step.

6. (Original) The process according to claim 5 wherein a basic encoding constraint for a minimum transition spacing is set to $2T_{channel}$, where $T_{channel}$ is a channel synchronization time unit.

7. (Currently Amended) The process according to claim 5 wherein said Viterbi detector supports twenty sequences with zero Running Digital Sum (RDS) for a six-bits sequence $cw=\{x_0, x_1, x_2, \ldots, x_5\}$ according to the following relationship:

$$RDS[cw] = \sum_{i=0}^{5}(-1)^{x[i]},$$

~~Such~~ such a six-bits sequence being in the 4/6 MSN code if RDS[cw]=0, thus enabling the design of the rate 4/6 code.

8. (Original) The process according to claim 5 wherein in said encoding step, each group of four bits of the pattern signal is switched into a six bit code according to the following assignments:

0000	001011
0001	001110
0011	011010
0010	010011
0110	010110
0111	011100
0101	001101
0100	011001
1100	110001
1101	010101
1111	110100
1110	100101
1010	101100
1011	100110
1001	100011
1000	101001

9. (Original) An encoding and decoding process for a servo positioning system of a reading and writing head of a hard disk drive, comprising the following steps:

receiving a pattern signal that includes a plurality of groups of four bits;

encoding each group of four bits of the pattern signal to a five bit code including a fifth final parity bit;

providing a biphase encoding of the five bit code to produce an encoded word that is written to a hard disk of the hard disk drive;

reading from the hard disk a servo wedge information signal, that includes the encoded word, using a read and write channel of the hard disk drive; and

using a trellis Partial Response decoding scheme matched to said encoded word for obtaining angular and radial information for positioning the head.

10. (Original) The encoding and decoding process according to claim 9, wherein each four-bit group $\{x_0\ x_1\ x_2\ x_3\}$ is encoded in a five-bit code $\{x_0\ x_1\ x_2\ x_3\ xp_4\}$ with xp_4 defined as:

$$xp_4 = [\sum_{i=0}^{3} xi\ ] \bmod 2 \qquad \text{with Xi = 0 or 1}$$

11. (Original) The encoding and decoding process according to claim 10, wherein said biphase encoding step is performed using a biphase map for each symbol xp_i.

12. (Original) The encoding and decoding process for a servo positioning system of a reading and writing head of a hard disk drive, comprising the following steps:

encoding a predetermined group of input bits of a pattern signal in a Matched Spectral Null (MSN) format through an intermediate rate 4/6 code to produce a six bit code word;

providing a duplicated bit for each bit of the six bit code word, thereby producing an encoded word that is written to a hard disk of the hard disk drive;

reading from the hard disk a servo wedge information signal, that includes the encoded word, using a read and write channel of the hard disk drive; and

using a trellis Partial Response decoding scheme matched to said encoded word for obtaining angular and radial information for positioning the head.

13. (Original) An encoding and decoding process for a servo positioning system of a reading and writing head of a hard disk drive, comprising the following steps:

receiving a pattern signal that includes a plurality of groups of four bits;

encoding each group of four bits of the pattern signal by adding a parity check bit as an intermediate rate 4/5 code;

encoding each of the five bits using a biphase map to produce an encoded word that is written to a hard disk of the hard disk drive;

reading from the hard disk a servo wedge information signal, that includes the encoded word, using a read and write channel of the hard disk drive; and

using a trellis Partial Response decoding scheme matched to said encoded word for obtaining angular and radial information for positioning the head.

14. (Original) A Viterbi data detector for encoding and decoding phases in a servo positioning system of a reading and writing head of a hard disk drive, said detector being associated with a reading and writing channel for picking-up servo wedges information from a hard disk of the hard disk drive, the data detector comprising:

means for receiving from said servo wedges information encoded through an intermediate 4/6 Matched Spectral Null (MSN) encoding phase followed by a duplication of each bit of six bit code word obtained with the encoding phase; and

a decoder including a trellis structure for obtaining from the servo wedges a partial response indicative of angular and radial information for positioning the head.

15. (Original) The data detector according to claim 14, wherein said trellis structure includes at least four Add, Compare and Select units (ACS) which are selectively assigned to different states according to a predetermined ACS rotation scheme.

16. (Original) The data detector according to claim 14, wherein a servo sync 16-bit binary pattern is used as servo wedge.

17. (Original) A Viterbi data detector for the encoding and decoding phases in a servo positioning system of a reading and writing head of a hard disk drive, said detector being associated with a reading and writing channel for picking-up servo wedges information from a hard disk of the hard disk drive , the data detector comprising:

means for receiving from said servo wedges information encoded through an intermediate 4/5 Parity Check encoding phase followed by a biphase encoding step of each bit of a five bit code word obtained with the previous phase; and

a decoder including a trellis structure for obtaining a partial response indicative of angular and radial information for positioning the head.

18. (New) The process according to claim 12 wherein the encoding phase is a concatenation of a 4/6 MSN encoding phase and a 1/2 repetition code.

19. (New) The process according to claim 12 wherein a 'gray-like' code feature is achieved by imposing a property of a minimum Euclidean distance between code words corresponding to two consecutive gray codes.

20. (New) The process according to claim 1 wherein the encoding step prevents MSN sequences such as '000111' and '111000' in order to minimize the number of trellis states.

21. (New) The process according to claim 12 wherein a sixteen states Viterbi detector is used for the decoding step.

22. (New) The process according to claim 21 wherein a basic encoding constraint for a minimum transition spacing is set to $2T_{channel}$, where $T_{channel}$ is a channel synchronization time unit.

23. (New) The process according to claim 21 wherein said Viterbi detector supports twenty sequences with zero Running Digital Sum (RDS) for a six-bits sequence $cw=\{x_0, x_1, x_2, \ldots, x_5\}$ according to the following relationship:

$$RDS[cw] = \sum_{i=0}^{5}(-1)^{x[i]},$$

such a six-bits sequence being in the 4/6 MSN code if RDS[cw]=0, thus enabling the design of the rate 4/6 code.

24. (New) The process according to claim 12 wherein in said encoding step, each group of four bits of the pattern signal is switched into a six bit code according to the following assignments:

0000	001011
0001	001110
0011	011010
0010	010011
0110	010110
0111	011100
0101	001101
0100	011001
1100	110001
1101	010101
1111	110100
1110	100101
1010	101100
1011	100110
1001	100011
1000	101001

25. (New) The encoding and decoding process according to claim 13, wherein each four-bit group $\{x_0\ x_1\ x_2\ x_3\}$ is encoded in a five-bit code $\{x_0\ x_1\ x_2\ x_3\ xp_4\}$ with xp_4 defined as:

$$xp_4 = [\sum_{i=0}^{3} xi\ ] \bmod 2 \qquad \text{with Xi = 0 or 1}$$

26. (New) The encoding and decoding process according to claim 25, wherein said biphase encoding step is performed using a biphase map for each symbol xp_i.

27. (New) The data detector of claim 17, further comprising an encoder that encodes an input four-bit group $\{x_0\ x_1\ x_2\ x_3\}$ to a five-bit code $\{x_0\ x_1\ x_2\ x_3\ xp_4\}$ with xp_4 defined as:

$$xp_4 = [\sum_{i=0}^{3} xi\ ] \bmod 2 \qquad \text{with Xi = 0 or 1.}$$

28. (New) The data detector of claim 27, wherein said encoder includes means for using a biphase map for each symbol xp_i.